IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1. (Currently Amended) A field effect transistor (FET) comprising:

a fin structure;

conducting spacers contacting said fin structure, wherein an upper surface of said conducting spacers is substantially planar with an upper surface of said fin structure;

an insulator contacting said spacers, wherein said insulator is structurally isolated from said fin structure; and

a gate layer positioned on top of and contacting said fin structure, said spacers, and said insulator.

2. (Original) The FET of claim 1, further comprising:

a substrate; and

an isolation layer positioned over said substrate,

wherein said isolation layer is positioned under said insulator, said spacers, and said fin structure.

3. (Original) The FET of claim 2, further comprising source/drain regions above said isolation layer.

PAGE 2/13 * RCVD AT 2/27/2006 7:40:04 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/24 * DNIS:2738300 * CSID:3012618825 * DURATION (mm-ss):03-18

4. (Original) The FET of claim 1, wherein said fin structure comprises an oxide layer over a silicon layer.

5. (Previously Presented) The FET of claim 1, further comprising an oxide layer contacting said fin structure.

6. (Original) The FET of claim 4, further comprising a second oxide layer over said oxide layer, wherein said second oxide layer is planar to said gate layer.

7. (Original) The FET of claim 1, wherein said spacers and said gate layer comprise the same material.

8. (Original) The FET of claim 7, wherein said material comprises polysilicon.

9. (Original) The FET of claim 1, further comprising a gate insulator positioned between said fin structure and said spacers.

10. (Previously Presented) The FET of claim 1, further comprising a second insulator contacting said insulator.

11. (Currently Amended) A field effect transistor (FET) device comprising:

a fin structure;

PAGE 3/13 * RCVD AT 2/27/2006 7:40:04 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/24 * DNIS:2738300 * CSID:3012618825 * DURATION (mm-ss):03-18

a first gate electrode contacting said fin structure;

a gate insulator positioned between said first gate electrode and said fin structure;

a second gate electrode positioned transverse to said first gate electrode; and

a third gate electrode positioned on top of and contacting said fin structure, said first gate electrode, and said second gate electrode.

12. (Original) The device of claim 11, further comprising:

a substrate; and

an isolation layer positioned over said substrate,

wherein said isolation layer is positioned beneath said gate insulator, said first gate electrode, and said fin structure.

13. (Original) The device of claim 12, wherein said isolation layer is isolated from said second gate electrode.

14. (Original) The device of claim 12, further comprising source/drain regions above said isolation layer.

15. (Original) The device of claim 11, further comprising a dielectric material sandwiching said second gate electrode.

16. (Original) The device of claim 11, wherein said fin structure comprises an oxide layer

PAGE 4/13 * RCVD AT 2/27/2006 7:40:04 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/24 * DNIS:2738300 * CSID:3012618825 * DURATION (mm-ss):03-18

over a silicon layer.

17. (Previously Presented) The device of claim 11, further comprising an oxide layer contacting said fin structure.

18. (Original) The device of claim 16, further comprising a second oxide layer over said oxide layer, wherein said second oxide layer is planar to said third gate electrode.

19. (Original) The device of claim 11, wherein said first gate electrode and said third gate electrode comprise the same material.

20. (Original) The device of claim 19, wherein said material comprises polysilicon.

21. (Currently Amended) A method of lowering a gate capacitance and extrinsic resistance in a field effect transistor (FET), said method comprising:

forming a fin structure;

configuring a first gate electrode contacting said fin structure;

disposing a gate insulator between said first gate electrode and said fin structure;

positioning a second gate electrode transverse to said first gate electrode; and

depositing a third gate electrode on top of and contacting said fin structure, said first gate electrode, and said second gate electrode.

PAGE 5/13 * RCVD AT 2/27/2006 7:40:04 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/24 * DNIS:2738300 * CSID:3012618825 * DURATION (mm-ss):03-18

22. (Original) The method of claim 21, further comprising forming an isolation layer over a substrate, wherein said isolation layer comprises a buried oxide (BOX) layer, and wherein said isolation layer is positioned beneath said gate insulator, said first gate electrode, and said fin structure.

23. (Original) The method of claim 22, further comprising configuring source/drain regions above said isolation layer.

24. (Original) The method of claim 21, further comprising sandwiching said second gate electrode with a dielectric material.

25. (Original) The method of claim 21, wherein said fin structure is formed by depositing an oxide layer over a silicon layer.

26. (Previously Presented) The method of claim 21, further comprising forming an oxide layer contacting said fin structure.

27. (Original) The method of claim 25, further comprising forming a second oxide layer over said oxide layer, wherein said second oxide layer is planar to said third gate electrode.

28. (Original) The method of claim 21, further comprising using the same material to form said first gate electrode and said third gate electrode.

BEST AVAILABLE COPY

29. (Original) The method of claim 28, wherein said material comprises polysilicon.

BEST AVAILABLE COPY

PAGE 7/13 * RCVD AT 2/27/2006 7:40:04 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/24 * DNIS:2738300 * CSID:3012618825 * DURATION (mm-ss):03-18